Eric Qian

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System Engineer with experience in embedded systems, OS firmware, low-level hardware abstractions, GPU architecture, and firmware/hardware debugging. Proven track record of collaborating with platform architecture to align product specifications, troubleshoot, and resolve product integration challenges.

Experience

Hardware Systems and Data Engineer ***[Apple Inc.]*** Sept. 2023 to Present

- ❏ Established power profile characterization and data infrastructure for Watch EE team, including hardware prototype bring-up.
- ❏ Orchestrated telemetry collection and analyzed large datasets to identify bug escapes and project field performance.
- ❏ Collaborated with product architecture and sensor teams to mitigate product-blocking issues.
- ❏ Built multithreaded and containerized backend with gRPC and FastAPI endpoints running on internal cloud. Created NextJS/ReactJS frontend with OIDC identity protocol, enabled highly reliable and scalable test infrastructure.
- ❏ Successfully resolved critical firmware issues involving C programming and custom ARM instruction sets.

Hardware Systems and Data Engineer, Intern ***[Apple Inc.]*** July 2022 to Dec. 2022

- ❏ Engineered automated UI test framework in Python, improving speed and coverage by over 200%.
- ❏ Created web-based visualization dashboard using NumPy and Plotly to analyze Power Management System efficacy and risks.
- ❏ Contributed to system integration tasks, system coexistence validation, and board component validation with GPIO, Serial, Oscilloscopes, and WaveGen.

Design Verification Engineer, Intern ***[Samsung Semiconductor LLC.]*** Q3 2021, Q2 2022

- ❏ Developed randomized UVM test benches written in C++ & SystemVerilog, increasing functional, toggle, and code coverage by over 60% for Samsung Exynos GPU's clock gating functionality.
- ❏ Designed React single-page application with NodeJS backend for dynamic data processing and parsing. Created debug GUIs that accelerate debug flow to correlate 5 independent ARM AMBA AXI & ACE data buses simultaneously using Tcl via Synopsys API.
- ❏ Collaborated with system architects to resolve critical design issues based on top-level + block-level test bench failures in DUT.

Education

California Polytechnic State University - San Luis Obispo Sept. 2019 to Sept. 2023

Bachelor of Science in Computer Engineering
Relevant Coursework: Operating Sys., Networks, Object Oriented Design, Data Structures, Microcontrollers, Assembly and Verilog, Computational Intelligence, Computer Architecture.
Teaching Assistant: Python Data Structure, EE Lab, MIPS Computer Architecture.

Projects

SORU - Self-supervised Original Response Uptake, A multimodal story generation framework May. 2023 to Aug. 2023

- ❏ Draft paper proposes a multimodal story generation framework with application of chaining an LLM to Stable Diffusion via template-based prompting and dynamically applying LoRA to create consistent character depictions across long contexts.

RISC-V RV32I MCU Implementation & MIPS Simulator - 32-bit interrupt-capable RISC-V MCU Sept. 2022 to Jan. 2023

- ❏ Implemented a fully functional interrupt-capable RISC-VMCU with 67 instructions, including function blocks such as PC, Memory, Registers, ALU, FSM, Instr Decoder, and Address Gen in Verilog.
- ❏ Utilized Xilinx Vivado and created numerous directed and constrained random simulation test benches for functional validation.
- ❏ Created MIPS Emulator in Python with dynamic branch prediction and pipeline stages. Also implemented a cache simulator that can model direct mapped and associative cache configurations with varying block sizes.

Trackversal - C, NodeJS, Express, MongoDB Nov. 2019 to Jun. 2023

- ❏ Founded a team for an IoT lost and found asset tracking device. Evaluated real-world technical feasibility and market demand.
- ❏ Developed backend API written in NodeJS with Express and MongoDB.
- ❏ Completed UART subsystem integration, sourced components, and optimized IoT power consumption by more than 75% via ISR and deep sleep via RTC.

Web Technologies: TypeScript, React, NodeJS, HTML, CSS, REST, OIDC, Cloud Infrastructure, Portainer, Load Balancer
Standalone Technologies: Python, C, Java, Linux/Embedded Linux, Tcl, Bash, Docker, Version Control (Git), VSCode, NumPy, Pandas
Hardware System Design: Eagle, SPICE, Verilog, Cura & Slic3r, STM32Cube/SEGGER Embedded Studio, Verdi, GPU Architecture
Organizations: Cal Poly CubeSat Laboratory, IEEE-HKN, Theta Tau, BananiumLabs, Inc., GLAARC VEC